

## **IIT Indore Patent Grant Press Note**

### **For Immediate Release:**

#### **CONTACT:**

**Contact Person-** Dr. Pooran Singh, Dr. Santosh Kumsr Vishvakarma

**Institution-** Indian Institute of Technology Indore

**Email Address-** [skvishvakarma@iiti.ac.in](mailto:skvishvakarma@iiti.ac.in)

**Website URL-** <https://sites.google.com/site/svishvakarma/>

### **Grant of Patent from Electrical Engineering Department, IIT Indore.**

#### **Details:**

**Indian Patent Application No.-** 201621038192

**Grant No.-** 370308

**Filing Date-** November 8, 2016

**Date of Grant-** June 25, 2021

**Title-** LOW LEAKAGE-HIGH STABILITY DIFFERENTIAL POSITIVE FEEDBACK CONTROLLED 10T (DPFC10T) SRAM CELL

**Inventors-** Pooran Singh, Santosh Kumar Vishvakarma

The IIT Indore patent on “LOW LEAKAGE-HIGH STABILITY DIFFERENTIAL POSITIVE FEEDBACK CONTROLLED 10T (DPFC10T) SRAM CELL” is granted by the Patent Office, Government of India. The inventors Dr. Pooran Singh and Prof. Santosh Kumar Vishvakarma from the Indian Institute of Technology Indore has proposed a novel static random-access memory (SRAM) for low power applications. The inventors impression is to develop a low power SRAM cell that works in subthreshold voltages (below the threshold voltage of transistor). The design is more suitable for ultra-low-power battery-operated wearable electronic devices such as wireless sensors, mobile or any other handheld devices. These days, microprocessor-controlled hand-held devices are comprised of embedded memory which characterizes a huge share of the system-on-chip (SoC). These hand-held systems require ultra-low power circuits to operate with the battery for a longer duration. Applications of ultra-low power SRAM are extremely broad including neural signal processor, sub-threshold processor, biomedical implants, wireless sensing, low voltage cache operation, etc. These applications demand careful design by maintaining the associated trade-off between power, stability and speed. In order to adhere to intense downscaling trends and the trade-off, a low power SRAM has been presented in our work.

**Dr. Pooran Singh** did his Ph.D. (2018) from the Department of Electrical Engineering, IIT Indore. Currently he is an Assistant Professor in the Electrical and Electronics Engineering Department at Mahindra University (MU) École Centrale School of Engineering.


Prior to joining MU, he was an Analog Design Engineer (SRAM Design) at Intel Microelectronics, Penang, Malaysia, his primary work included designing SRAM circuits, Pre-layout SRAM design and analysis of its various design parameters.

**Dr. Santosh Kumar Vishvakarma** is with the Department of Electrical Engineering, [Indian Institute of Technology Indore](#), MP, India as an Associate Professor. He is engaged with teaching and research in the area of Energy-Efficient and Reliable SRAM Memory Design, Enhancing Performance and Configurable Architecture for DNN Accelerators, SRAM based In-Memory Computing Architecture for Edge AI, Reliable, Secure Design for IoT Application, Design for Reliability.

Dr. Vishvakarma obtained Ph.D. degree on the topic "Analytical Modeling of Low Leakage MGDG MOSFET and its Application to SRAM" from Microelectronics and VLSI Group, Department of Electronics and Computer Engineering, [Indian Institute of Technology, Roorkee \(IITR\)](#) in 2010.



**INTELLECTUAL  
PROPERTY INDIA**  
PATENTS | DESIGNS | TRADE MARKS  
GEOGRAPHICAL INDICATIONS



भारत सरकार  
**GOVERNMENT OF INDIA**  
पेटेंट कार्यालय  
**THE PATENT OFFICE**  
पेटेंट प्रमाणपत्र  
**PATENT CERTIFICATE**  
(Rule 74 of The Patents Rules)


संख्यांक : 02213794  
SL No :




  

पेटेंट नं. / Patent No.	:	370308
अवेदन नं. / Application No.	:	201621038192
आवक करने की तारीख / Date of Filing	:	08/11/2016
पेटेंटी / Patentee	:	INDIAN INSTITUTE OF TECHNOLOGY INDORE
आविष्कारक (एक या अधिक) / Inventor(s)	:	1.Singh Pooran 2.Vishvakarma Santosh Kumar

प्रमाणित किया जाता है कि पेटेंटी को उपरोक्त आवेदन से सम्बन्धित LOW LEAKAGE-HIGH STABILITY DIFFERENTIAL POSITIVE FEEDBACK CONTROLLED 10T (DPFC10T) SRAM CELL नामक आविष्कार के लिए, पेटेंट अधिनियम, 1970 के प्रावधानों के अनुसार आज तारीख 8th day of November 2016 से बीस वर्ष की अवधि के लिए पेटेंट प्रदान किया गया है।  
 It is hereby certified that a patent has been granted to the patentee for an invention entitled LOW LEAKAGE-HIGH STABILITY DIFFERENTIAL POSITIVE FEEDBACK CONTROLLED 10T (DPFC10T) SRAM CELL as disclosed in the above mentioned application for the term of 20 years from the 8th day of November 2016 in accordance with the provisions of the Patents Act,1970.



**INTELLECTUAL  
PROPERTY INDIA**  
PATENTS | DESIGNS | TRADE MARKS  
GEOGRAPHICAL INDICATIONS

  
पेटेंट नियंत्रक  
Controller of Patent

दिल्ली - इस पेटेंट के नवीकरण से इस दिनांक, अर्थात् 08 दिनांक नवंबर 2016 के अगले तारीख तक प्रवृत्त रहे।  
 Delhi - The fee for renewal of this patent, if it is to be maintained will fall / has fallen due on 08th day of November 2016 and on the same day in every year thereafter.

