PRESS RELEASE: The Patent Office, Government of India has granted IIT Indore a patent for memory design.

The Indian patent office has granted IIT Indore patent on "**P-N tuned Differential 8T Static Random Access Memory (SRAM) cell".** The invention relates generally to integrated circuits, and more particularly to ultra-low power SRAM. In order to reduce the power consumption in a memory cell array, supply voltage scaling is the most preferred way. Supply voltage scaling enables the operation in sub-threshold regime, wherein there will be minimum power consumption by the circuit. It is achieved by selecting the supply voltage below the threshold voltage of the metal-oxide-semiconductor field-effect-transistor (MOSFET) device used. Supply voltage scaling through VLSI design comes with the constraints such as apparent loss in Static Noise Margin (SNM), current fluctuations, restraining the number of cells that may be connected to a single bit-line. The invention reduces the read-disturb and improve the write-ability of SRAM cell so as to operate the same more efficiently in ultra-low power operations. This invention also enhances the immunity of SRAM cell with process-voltage-temperature variations in sub-threshold region. This is achieved by cutting the feedback and restricting the current through true storage node to ground, thereby improving the write-ability and write speed of 8T SRAM cell allows setting a common write pulse width, improving writing speed. The absence of direct disturbance on true storage node during read operation, results in the reduction of failure probability under inter or intra die variations. This novel SRAM cell will enable the designers to build a robust memory array.

Patent details

Title: P-N TUNED DIFFERENTIAL 8T STATIC RANDOM ACCESS MEMORY (SRAM) CELL

Patent No.: 406860

Application No.: 2860/MUM/2015

Date of Filing: 28/07/2015

Patentee: Indian Institute of Technology Indore

Inventor(s): KUSHWAH CHANDRABHAN, VISHVAKARMA SANTOSH KUMAR

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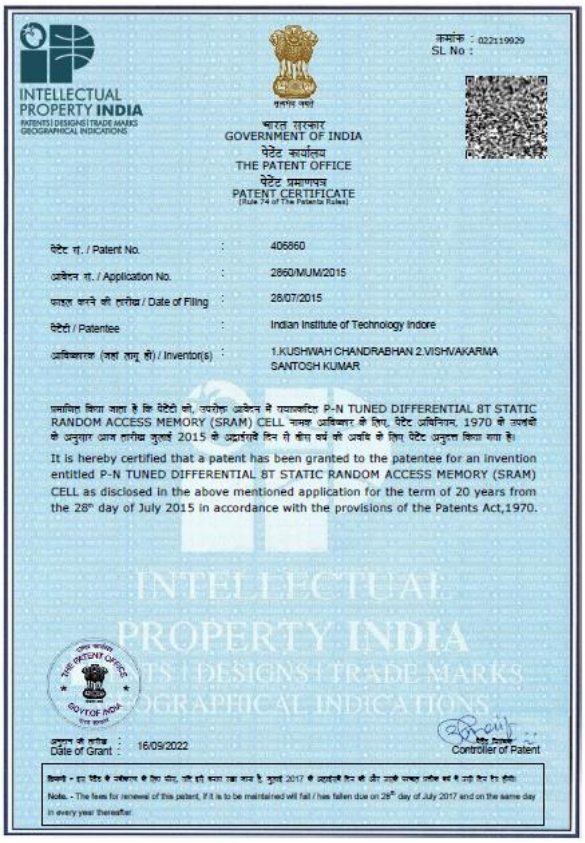
Patent Certificate



INTELLECTUAL PROPERTY INDIA
PATENTS | DESIGNS | TRADE MARKS
GEOGRAPHICAL INDICATIONS

कर्मांक : 022119929
SL No :

भारत सरकार
GOVERNMENT OF INDIA
पेटेंट कार्यालय
THE PATENT OFFICE
पेटेंट प्रमाणपत्र
PATENT CERTIFICATE
(Rule 74 of The Patents Rules)

पेटेंट सं. / Patent No.	:	406860
आवेदन सं. / Application No.	:	2860/MUM/2015
फाइल करने की तारीख / Date of Filing	:	28/07/2015
पेटेंटी / Patentee	:	Indian Institute of Technology Indore
आविष्कारक (कों) / Inventor(s)	:	1.KUSHWAH CHANDRABHAN 2.VISHVAKARMA SANTOSH KUMAR

प्रमाणित किया जाता है कि पेटेंटी को, उपरोक्त आवेदन में यथाप्रकटित P-N TUNED DIFFERENTIAL 8T STATIC RANDOM ACCESS MEMORY (SRAM) CELL नामक आविष्कार के लिए, पेटेंट अधिनियम, 1970 के उपबंधों के अनुसार आज तारीख जुलाई 2015 के अट्ठाईसवें दिन से बीस वर्ष की अवधि के लिए पेटेंट अनुदत्त किया गया है।

It is hereby certified that a patent has been granted to the patentee for an invention entitled P-N TUNED DIFFERENTIAL 8T STATIC RANDOM ACCESS MEMORY (SRAM) CELL as disclosed in the above mentioned application for the term of 20 years from the 28th day of July 2015 in accordance with the provisions of the Patents Act,1970.

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THE PATENT OFFICE GOVT OF INDIA

अनुदान की तारीख : 16/09/2022
Date of Grant :

Controller of Patent

टिप्पणी - इस पेटेंट के अधिकार के लिए फीस, जो देय करना रखा जाना है, जुलाई 2017 के अट्ठाईसवें दिन को और उसके पश्चात प्रत्येक वर्ष में उसी दिन देय होगी।
Note. - The fees for renewal of this patent, if it is to be maintained will fall / has fallen due on 28th day of July 2017 and on the same day in every year thereafter.

About the inventors

Dr. Chandrabhan Singh Kushwah is Postdoctoral Researcher at University of Manchester, United Kingdom, working on artificial neural network chip design for FORTE project. He was developing implantable wireless Adaptive Pacemaker system for H2020 project CResPace- for Chronic Cardiorespiratory Disease at University of Bath, UK. He has contributed to the field of Bio-inspired VLSI design and SRAM optimisation at University of York, UK. At IBM he invented novel SRAM architecture as a PhD fellow. He has given his services as guest lecturer at NIT Hamirpur and SGSITS Indore, India. He has earned his PhD from Indian Institute of Technology Indore where he was involved in designing Ultra-low Power SRAM.

Dr. Santosh Kumar Vishvakarma is a Professor in the Department of Electrical Engineering, Indian Institute of Technology Indore, MP. He is engaged in teaching and research in the area of Energy-Efficient and Reliable SRAM Memory Design, Enhancing Performance and Configurable Architecture for DNN Accelerators, SRAM-based In-Memory Computing Architecture for Edge AI, Reliable, Secure Design for IoT Application, Design for Reliability. Dr. Vishvakarma obtained a Ph.D. degree on the topic from Microelectronics and VLSI Group, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee (IITR) in 2010.